I²C protocol for EPT31LE pressure sensor

Variohm Eurosensor

1. Basis of serial communication via I²C

The pressure transmitter with I²C interface operates as a SLAVE on the I²C bus using the default slave address “0x78”.

2. I²C communication via I²C

On the SCL line, a clock signal must be generated by the master. The SDA line data is transmitted from master to slave or vice versa, the communication is controlled by the master.

2.1 BASICS

- **Idle time**
  While the bus is inactive, SDA and SCL are set to “high“ = to draw VDDa
- **Start condition**
  A high-to-low transition on SDA and SCL high to define a start of communication, each instruction of the master must be initiated by a start condition
- **End condition**
  A low-to-high transition on SDA and SCL high to define a start of communication, each instruction of the master must be terminated by a start condition

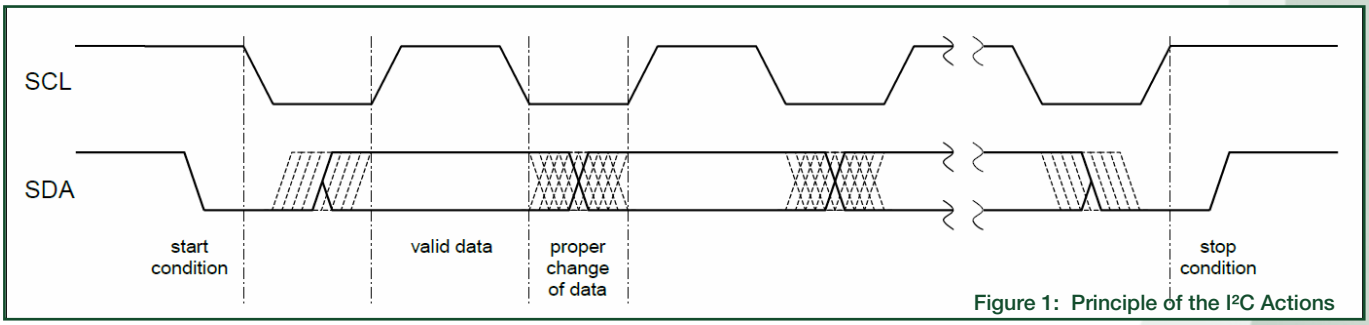


Figure 1: Principle of the I²C Actions

- **Valid Date**
  Data are transmitted starting with MSB in byte (8 bits). There are 16 bits of data which transmitted with a “high byte“ start (= “Big Endian“). After each transmitted byte acknowledge bit is transmitted. Total bytes transferred are correct, when, after a START condition SCL SDA remains the same while on high is. SDA is allowed to change only when SCL is low.
- **Acknowledge (ACK)**
  An ACK is required for byte transmitted. The master must generate an SCL to signal an ACK. The receiver (master or slave) takes a pull down SDA during.
- **Adressing**
  Each SLAVES connected to the I²C bus responds to a specific address. After the starting condition of the master, it sends the address byte (7bit) followed direction bit (R / W). By “0“ transmission from the master to SLAVE (“WRITE“) is characterized by “1“, a read operation is defined. The addressed slave sends an ACK, all other connected SLAVE ignore the command.
  The default address is “OX78”
- **Read Operation**
  After a REQUEST has been sent to the SLAVE with SLAVE address with direction from BIT MASTER, SLAVE will respond with the data. The data is transferred from the activated registers. The master then must generate data (except for the last) and the stop condition on the clock SCL that after each ACK byte.
  The data is continuously transferred until a STOP condition has been received.
  During this time the data in SIF (Serial Interface) are updated.

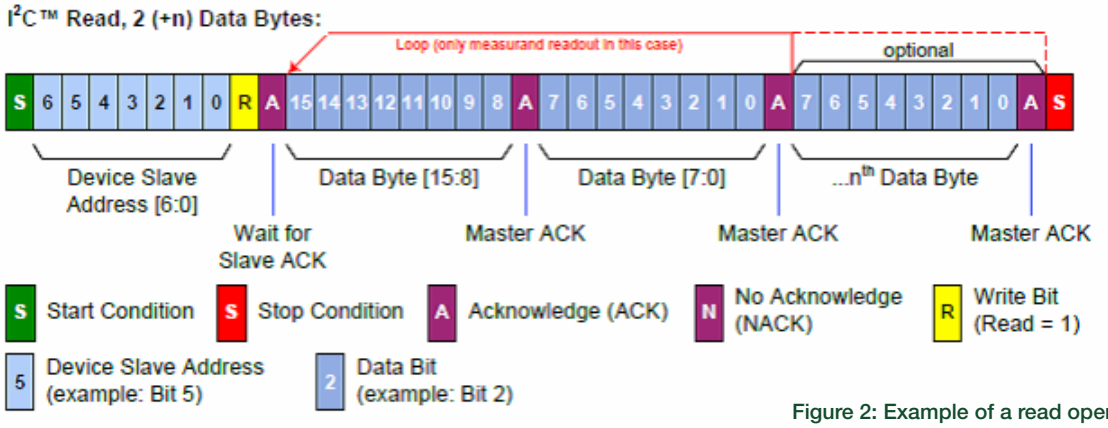
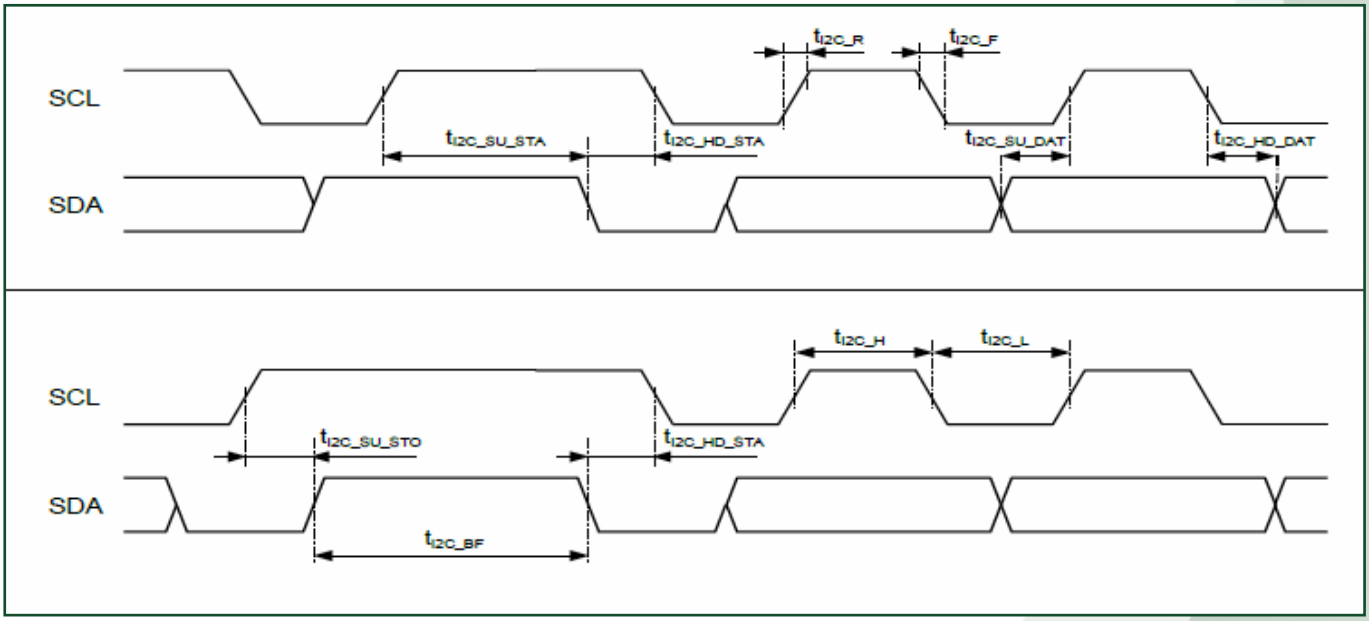


Figure 2: Example of a read operation

2.2 Timing



Nr.	Parameter	Symbol	min	typ	Max	Unit	Conditions
1	SCL clock frequency *	f_{SCL}			400	kHz	$f_{OSC} \geq 2MHz$
2	Bus free time between start and stop condition	t_{I2C_BF}	1.3			µs	
3	Hold time start condition	$t_{I2C\_HD\_STA}$	0.6			µs	
4	Setup time repeated start condition	$t_{I2C\_SU\_STA}$	0.6			µs	
5	Low period SCL/SDA	t_{I2C_L}	1.3			µs	
6	High period SCL/SDA	t_{I2C_H}	0.6			µs	
7	Data hold time	$t_{I2C\_HD\_DAT}$	0			µs	
8	Data setup time	$t_{I2C\_SU\_DAT}$	0.1			µs	
9	Rise time SCL/SDA	t_{I2C_R}			0.3	µs	
10	Fall time SCL/SDA	t_{I2C_F}			0.3	µs	
11	Setup time stop condition	$t_{I2C\_SU\_STO}$	0.6			µs	
12	Noise interception SDA/SCL	t_{I2C_NI}			50	ns	Spike suppression

Figure 3: I²C ™ timing protocol

2.3 Electrical connection

To avoid voltage spikes, resistors should be provided in the leads to the bus stations, additional pull-up resistors are required. The dimension of the resistance Rs and Rp depends inter alia on the cable capacity.

The bus capacity should not exceed 400µC. The slope of 300ns must be adhered to.

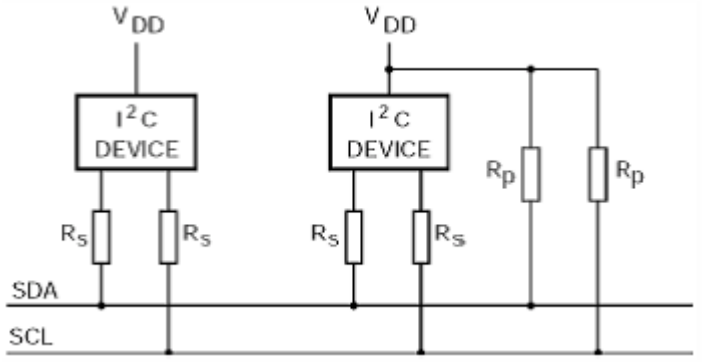


Figure 4: I2C-bus with a protection resistor RS in the leads of the bus devices

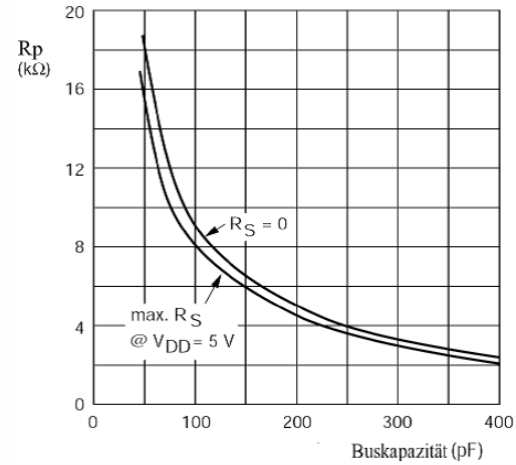


Figure 5 Size of the pull-up resistor RP as a function of bus capacitance

3. Available signal and / or range

Signal coding	Range
I2C	1000 – 30000 digits

Example:

a. EPT31LE (0-25) bar➜0bar = 1000digits, 12bar = 14920digits, 25bar = 30000digits

lit. ref to I2C spec: http://www.nxp.com/documents/user_manual/UM10204.pdf